a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed over said plug;

a predetermined void between said plug and said second interconnection; and

a second dielectric film covering said second interconnection.

A2 cancel

6. (Amended) A semiconductor device comprising:

a substrate;

a first interconnection formed on said substrate;

a first dielectric film covering said first interconnection;

an opening section extending from a surface of said first dielectric film to said first interconnection, said opening section being formed in said first dielectric film;

a plug formed in said opening section and electrically connected to said first interconnection;

a second interconnection formed on said first dielectric film in the vicinity of said plug ;

a second dielectric film covering said second interconnection; and

a predetermined void in said second dielectric film and located at a position adjacent to said second interconnection and at a position above said plug.

A3

15. (Amended) A semiconductor device comprising:

a substrate;

a first dielectric film formed on said substrate and having an opening section;

a pad formed in the opening section and having conductivity;

a3 cont.

a first interconnection formed on said first dielectric film such that a portion of a bottom of said first interconnection comes into contact with an upper surface of said pad;

a second interconnection formed on said first dielectric film such that a bottom surface of said second interconnection does not come into contact with the upper surface of said pad, said pad being disposed between said first and second interconnections; and

a second dielectric film covering said first and second interconnections; and

a predetermined void in said second dielectric film and located at a position on said pad.

REMARKS

At the time of the Office Action dated June 5, 2002, claims 1-18 were pending in this application. On page one of the "Office Action Summary," the Examiner indicated that claims 1-18 are rejected. However, in the "Detailed Action," the Examiner only provided rejections for claims 1-6 and 15. As such, the Examiner has failed to indicate a basis for rejecting claims 7-14 and 16-18. Therefore, if the Examiner is to issue a second Office Action, the second Office Action cannot be made final.

In the first enumerated paragraph of the Office Action, the Examiner objected to the drawings pursuant to 37 C.F.R. § 1.83(a), requiring that a load circuit and a short circuit or spare circuit be shown or deleted from the claims. In response, Applicant notes that these features have been deleted from independent claims 1, 6, and 15. As such, the Examiner's objection has been rendered moot.